



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,999	04/15/2004	Rocky R. Arnold	020843-002810US	9224

20350 7590 09/06/2006

TOWNSEND AND TOWNSEND AND CREW, LLP  
TWO EMBARCADERO CENTER  
EIGHTH FLOOR  
SAN FRANCISCO, CA 94111-3834

EXAMINER

CARPIO, IVAN HERNAN

ART UNIT

PAPER NUMBER

2841

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/825,999

Applicant(s)

ARNOLD ET AL.

Examiner

Ivan H. Carpio

Art Unit

2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE \_\_\_\_\_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-38 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/21/04</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1- are rejected under 35 U.S.C. 102(b) as being anticipated by Higgins III (US Patent 5639989).

With respect to claim 1 Higgins teaches a shielded printed circuit board (PCB) (Fig.1) comprising: a PCB comprising a first surface and a second surface; a metallized polymer shield (Fig. 1, element 24 with 26) coupled to the first surface of the PCB; a grounded layer (Fig. 1, element 27) coupled to the second surface of the PCB; and a plurality of conductive vias (Fig. 1, element 20) that extend from the first surface to the grounded layer so as to electrically couple the metallized polymer shield to the grounded layer.

With respect to claims 2 and 18 with all the limitations of claims 1 and 15 respectively, Higgins teaches comprising an electronic component (Fig. 1, element 13) mounted to the first surface of the PCB, wherein adjacent conductive vias are spaced within the PCB a distance that is small enough to reduce a passage of electromagnetic radiation from the electronic component through the spacing between the adjacent

conductive vias (Note this true because of the EMI ground layer, the spacing is sufficiently small along with the EMI ground layer to reduce passage of electromagnetic radiation).

With respect to claim 3 and with all the limitations of claim 1, Higgins teaches an electronic component mounted to the first surface of the PCB, wherein the plurality of conductive vias, grounded layer, and metallized polymer shield forms a three dimensional grounded EMI shield that substantially envelopes the electronic component (Fig. 1).

With respect to claim 4 and with all the limitations of claim 1, Higgins teaches that the metallized polymer shield is removably coupled to the first surface of the PCB (Fig. 1).

With respect to claim 5 and with all the limitations of claim 4, Higgins teaches that the metallized polymer shield is coupled to the vias through a conductive element (Fig. 1, elements 19 and 18).

With respect to claims 6 and 21 and with all the limitations of claim 5, Higgins teaches that the conductive element comprises a conductive adhesive (Fig. 1, element 19).

With respect to claims 7 and 20 with all the limitations of claims 4 and 15 respectively, Higgins teaches the metallized polymer shield is coupled to the vias through a mechanical connector (Fig. 1, the land portion of the via 20).

With respect to claim 8 and with all the limitations of claim 1, Higgins teaches that the PCB comprises two or more layers, wherein the second surface is between two adjacent layers of the PCB (Fig. 1).

With respect to claim 9 and with all the limitations of claim 1, Higgins teaches that the second surface is an external, bottom surface of the PCB (note the ground plane is coupled to the bottom surface).

With respect to claim 10 and with all the limitations of claim 1, Higgins teaches that the grounded layer comprises a ground plane (Fig.1, element 27).

With respect to claim 11 and with all the limitations of claim 1, Higgins teaches that the grounded layer is electrically coupled to a ground plane.

With respect to claim 14 and with all the limitations of claim 1, Higgins teaches an electronic device

With respect to claim 15 Higgins teaches a printed circuit board (Fig. 1) comprising: a multi-layered substrate that comprises a first external surface and a second external surface, wherein a portion of the first external surface is configured to receive an electronic component (Fig. 1, element 13); one or more internal grounded layers (Fig. 1, element 27) disposed between adjacent layers of the multi-layered substrate; a network of conductive elements (Fig. 1, elements 20) that extend through at least a portion of the multi-layered substrate, wherein the electrically conductive elements extend from at least one of the internal grounded planes to the first external surface; and a shield coupled (Fig.1, element 24 with 26) to the first surface, the shield electrically coupled to at least some of the conductive elements to provide an electrical

grounding connection between the shield and the one or more internal grounded planes.

With respect to claim 16 and with all the limitations of claim 15, Higgins teaches that the network of conductive elements comprises a plurality of conductively coated (Fig. 1, element 20).

With respect to claim 17 and with all the limitations of claim 15, Higgins teaches a grounding trace (Fig. 1, element 20) on the first external surface that substantially surrounds the portion of the first external surface that is configured to receive an electronic component.

With respect to claim 22 and with all the limitations of claim 20, Higgins teaches that the mechanical connector comprises a groove (Fig. 1, the space between the lands of vias 20) in the first surface, wherein the groove is sized to receive a portion of an EMI shield.

With respect to claim 25 and with all the limitations of claim 15, Higgins teaches that the shield is coupled to a ground trace positioned on the first external surface, wherein the ground trace is in electrical communication with at least some of the conductive elements (Fig. 1).

With respect to claim 26 and with all the limitations of claim 15, Higgins teaches that the conductive elements (Fig. 1, element 20) make direct contact with a flange of the shield (Fig. 1, element 19).

With respect to claim 27 and with all the limitations of claim 26, Higgins teaches a conductive element (Fig. 1, the land portion of 20) is disposed on a portion of the

Art Unit: 2841

conductive elements (Fig.1, elements 20) to create an electrical connection to the shield positioned on the first external surface.

With respect to claim 28 and with all the limitations of claim 26, Higgins teaches that the conductive element (Fig. 1, element 20) comprises conductive adhesive.

With respect to claim 29 and with all the limitations of claim 15, Higgins teaches an electronic device (Fig. 1) comprising the PCB of claim 15.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins.

With respect to claim 12 and 24 with all the limitations of claim 1 and 15 respectively, Higgins teaches all of the limitations except that a metal layer is disposed over at least one surface of the shaped polymer substrate. Metal layers in the shielding art and PCB art are well known, they are used for the shielding itself or for structural support. It would have been obvious to one of ordinary skill in the art at the time of the invention add a metal layer disposed on a surface of the shaped polymer substrate for the purpose of adding structural strength while increasing the shielding capability of the structure.

With respect to claim 13 and with all the limitations of claim 1, Higgins teaches all of the limitations except for that the flange comprises openings. When attaching a component to a circuit board we need the component connectors to make physical contact with the vias structures on the board, in order to do this there must be openings in any material that covers the vias. It would have been obvious to one of ordinary skill in the art at the time of the invention to have openings on the flange for the purpose of attaching more components to the vias underneath.

With respect to claim 23 and with all the limitations of claim 15, Higgins teaches all of the limitations except that the shield comprises a metal can. Metal cans are well known in the shielding art and are used in various realms to shield devices from EMI emissions while at the same time providing structural strength for physical protection of the device. It would have been obvious to one of ordinary skill in the art at the time of the invention add a metal can disposed on a surface of the shaped polymer substrate for the purpose of adding structural strength while increasing the shielding capability of the structure.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins in view of Kaneko (US Patent 6476463).

With respect to claim 19 and with all the limitations of claim 18, Higgins teaches all of the limitations except does not teach specifically that the largest dimension is smaller than half a wavelength of EMI emissions from the electronic component. Kaneko teaches vias that are separated by certain dimensions wherein the largest dimension is smaller than half a wavelength of EMI emissions from the electronic



Art Unit: 2841

component (column 5, lines 13-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the largest dimension separating vias to be smaller than half a wavelength of EMI emissions from the electronic component, for the purpose of quickly attenuating the EMI emissions.

### ***Conclusion***

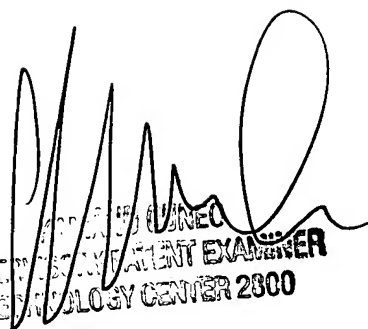
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ivan H. Carpio whose telephone number is 571-272-8396. The examiner can normally be reached on M-R 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Art Unit: 2841

IC

  
SUPERVISOR  
TECHNOLOGY CENTER 2800